IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. **BUR920020055US1**

In re Application of:

HAYES ET AL.

Serial No.: **10/604,107**

Filed: **26 JUNE 2003**

For: **METHOD AND APPARATUS FOR PERFORMING INPUT/OUTPUT FLOOR PLANNING ON AN INTEGRATED CIRCUIT DESIGN**

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Confirmation No.: **1106**

Examiner: **PIERRE LOUIS, A.**

Art Unit: **2123**

APPEAL BRIEF

MS Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The present Brief is submitted in support of the Appeal in the above-identified application.

Please charge IBM Corporation Deposit Account **09-0456** in the amount of $500.00 for the submission of the present Brief. No additional fee or extension of time is believed to be required; however, in the event an additional fee or extension of time is required, please charge that fee to the IBM Corporation Deposit Account **09-0456**.

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REAL PARTY IN INTEREST

The present application is assigned to International Business Machines Corporation, the real party of interest.

RELATED APPEALS AND INTERFERENCES

No related appeal is presently pending.

STATUS OF THE CLAIMS

Claims 1-12, which were finally rejected by the Examiner as noted in the Final Office Action dated May 18, 2006 and in the Advisory Action dated August 2, 2006, are being appealed.

STATUS OF AMENDMENTS

An Amendment submitted on July 21, 2006 in reply to the Final Office Action dated May 18, 2006 was not entered.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The claimed invention is related to a method for performing input/output (I/O) floor planning on an integrated circuit design. According to Claim 1 (and similarly Claim 5), user design data related to I/O circuits associated with each package pin are initially collected (paragraph 0026, lines 3-5; block **51** of Figure **5**). The collected user design data is then sorted according to predetermined operating conditions (paragraph 0026, lines 6-7; block **52** of Figure **5**). Next, a determination is made as to whether or not a simulation is required for the I/O circuit before performing I/O floor planning on the I/O circuit (paragraph 0026, lines 8-10; block **53** of Figure **5**).

If a simulation is required on the I/O circuit before performing I/O floor planning on the I/O circuit, the collected design data are sent to a simulation interface, an I/O behavioral model and a package model are chosen by the simulation interface based on the collected design data on the I/O circuit, and a simulation deck is dynamically built by the simulation interface using

the chosen models along with appropriate operating conditions (paragraph 0027, lines 1-3; block 55 of Figure 5).

The simulation results are received by the simulation interface from a circuit simulator after a simulation has been performed by the circuit simulator using the simulation deck that contains the chosen I/O behavioral model and the operating conditions (paragraph 0027, lines 4-7; block 56 of Figure 5). Finally, an I/O floor planning is performed for the I/O circuit, according to the received simulation results.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Examiner's rejection of Claim 9 under 35 U.S.C. § 101 as being non-statutory subject matter.

The Examiner's rejection of Claim 9 under 35 U.S.C. § 112, first paragraph, as not complying with the enablement requirement.

The Examiner's rejections of Claims 1-2, 4-6, 8-10 and 12 under 35 U.S.C. § 102(b) as being anticipated by *Rostoker et al.* (US 5,557,531).

The Examiner's rejections of Claims 3, 7, and 11 under 35 U.S.C. § 103(a) as being unpatentable over *Rostoker et al.* (US 5,557,531) in view of *Chang et al.* (US 6,269,467).

ARGUMENT

The Examiner's rejections of Claims 1-12 were not well-founded and should be reversed.

I.   The Examiner has no basis for not entering the Amendment after Final

In response to the Final Office Action dated May 18, 2006, an Amendment after Final was submitted on July 21, 2006 to cancel Claims 9-12 without adding any new matters. As such, the above-mentioned Amendment after Final did not raise any new issues that would require further search. In fact, because of the proposed claim cancellation, the above-mentioned Amendment

after Final would place the application in better form for appeal by reducing issues for appeal, such as rejections on Claim 9 under 35 U.S.C. §§ 101, 112, first paragraph. Thus, it was improper for the Examiner not to enter the above-mentioned Amendment after Final.

The Appellants have included another Amendment after Final with the present Appeal Brief for cancelling Claims 9-12. According, the Appellants maintain the position that rejections on Claim 9 under 35 U.S.C. §§ 101, 112, first paragraph, are moot on the basis that Claim 9 has been requested to be cancelled.

II.   _Rostoker_ does not teach or suggest the claimed sending, choosing, building and receiving steps in response to a determination that a simulation is required on an I/O circuit before performing I/O floor planning on the I/O circuit

Claim 1 (and similarly Claim 5) recites "determining whether or not a simulation is required for said I/O circuit before performing I/O floor planning on said I/O circuit," and "in response to a determination that a simulation is required on said I/O circuit before performing I/O floor planning on said I/O circuit,

> sending said collected design data to a simulation interface;

> choosing an I/O behavioral model and a package model by said simulation interface based on said collected design data on said I/O circuit;

> dynamically building a simulation deck by said simulation interface using said chosen models along with appropriate operating conditions; and

> receiving simulation results by said simulation interface from a circuit simulator after a simulation had been performed by said circuit simulator using said simulation deck containing said chosen I/O behavioral model and said operating conditions."

Thus, according to the claimed invention, a determination is initially made as to whether or not a simulation is required for an I/O circuit before performing I/O floor planning on the I/O circuit. If a simulation is required, then the collected design data is sent to a simulation interface. Within the simulation interface, an I/O behavioral model and a package model are chosen "based on said collected design data on said I/O circuit," a simulation deck is dynamically builded "using said chosen models along with appropriate operating conditions." A simulation is then performed using the "simulation deck containing said chosen I/O behavioral model and said operating conditions." The I/O floor planning is subsequently performed for the I/O circuit based on the received simulation results.

Rostoker does not teach or suggest the above-mentioned claimed steps. For example, on page 4 of the Final Office Action, the Examiner asserts that the claimed determining step is disclosed by *Rostoker* in col. 1, line 33 - col. 6, line 5 and in col. 7, line 55 - col. 15, line 27. Although the Examiner has cited almost half of the length of the reference to show one claimed step, the claimed determining step is still not disclosed in the cited passages as evidenced by the fact that none of Figures **2-9** and **18** discloses a decision step, much less the claimed determining step.

On page 4 of the Final Office Action, the Examiner again asserts that the same cited passages of *Rostoker* (*i.e.*, col. 1, line 33 - col. 6, line 5 and in col. 7, line 55 - col. 15, line 27) disclose the claimed choosing step, the claimed building step and the claimed receiving step. Assuming *arguendo* that *Rostoker* may have disclosed one or more of the claimed choosing, building and receiving steps in various portions of the above-cited passages, but *Rostoker* does not teach or suggest that the claimed choosing, building and receiving steps being performed together after a determination that a simulation is required. As mentioned above, *Rostoker* does not teach or suggest such a determination step; thus, it is clear that even if *Rostoker* does disclose one or more of the claimed choosing, building and receiving steps, they are not performed "in response to a determination that a simulation is required on said I/O circuit before performing I/O floor planning on said I/O circuit," as claimed. Because the present invention recites novel features that are taught or suggested by *Rostoker*, the § 102 rejection is improper.

III.   *Chang* does not teach or suggest collecting design specification from a customer's environment condition

Claim 3 (and similarly Claim 7) recites a step of "collecting design specification from a customer's environment condition." On page 6 of the Final Office Action, the Examiner asserts that the claimed collecting step is disclosed by *Chang* in Figure 2. Only one block in *Chang*'s Figure 2 mentions "customer data & specification," and such block does not teach or suggest "collecting design specification <u>from a customer's environment condition</u>" (emphasis added).

In addition, the Examiner also asserts that the claimed collecting step is disclosed by *Chang* in col. 1, line 17 - col. 4, line 65 and in col. 7, line 63 - col. 9, line 64. Col. 1, line 17 - col. 4, line 65 explain the background of the invention, and col. 7, line 63 - col. 9, line 64 are related to Figure 1, but neither of the cited section teaches or suggests the claimed collecting step. According to 37 C.F.R. § 1.104 (c)(2), when a reference shows inventions other than that claimed by the Appellants, the particular part relied on by the Examiner for the obviousness rejection must be designated as nearly as practicable. The Examiner has not done so. Because the cited references, whether considered separately or in combination, do not teach or suggest the claimed invention, the § 103 rejection is improper.

CONCLUSION

For the reasons stated above, Appellants believe that the claimed invention clearly is patentably distinct over the cited reference, and that the rejections under 35 U.S.C. §§ 102, 103 are not well-founded. Hence, Appellants respectfully urge the Board to reverse the Examiner's rejection.

Respectfully submitted,

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ATTORNEY FOR APPELLANTS

CLAIMS APPENDIX

1.   A method for performing input/output (I/O) floor planning on an integrated circuit design, said method comprising:

collecting design data related to an I/O circuit of said integrated circuit design from a plurality of libraries, customer specifications and design databases;

sorting said collected design data for optimizing simulations of said I/O circuit under operating conditions;

determining whether or not a simulation is required for said I/O circuit before performing I/O floor planning on said I/O circuit;

in response to a determination that a simulation is required on said I/O circuit before performing I/O floor planning on said I/O circuit,

sending said collected design data to a simulation interface;

choosing an I/O behavioral model and a package model by said simulation interface based on said collected design data on said I/O circuit;

dynamically building a simulation deck by said simulation interface using said chosen models along with appropriate operating conditions; and

receiving simulation results by said simulation interface from a circuit simulator after a simulation had been performed by said circuit simulator using said simulation deck containing said chosen I/O behavioral model and said operating conditions; and

performing I/O floor planning for said I/O circuit based on said received simulation results.

2.   The method of Claim 1, wherein said method further includes dynamically analyzing simulation results based on user defined criteria.

3.   The method of Claim 1, wherein said collecting further includes collecting design specification from a customer's environment condition.

4.   The method of Claim 1, wherein said sorting further includes sorting said collected design data according to a frequency of operation of said I/O circuit.

5.   A system for performing input/output (I/O) floor planning on an integrated circuit design, said system comprising:

          means for collecting design data related to an I/O circuit of said integrated circuit design from a plurality of libraries, customer specifications and design databases;

          means for sorting said collected design data for optimizing simulations of said I/O circuit under operating conditions;

          means for determining whether or not a simulation is required for said I/O circuit before performing I/O floor planning on said I/O circuit;

          in response to a determination that a simulation is required on said I/O circuit before performing I/O floor planning on said I/O circuit,

               means for sending said collected design data to a simulation interface;

means for choosing an I/O behavioral model and a package model by said simulation interface based on said collected design data on said I/O circuit;

means for dynamically building a simulation deck by said simulation interface using said chosen models along with appropriate operating conditions; and

means for receiving simulation results by said simulation interface from a circuit simulator after a simulation had been performed by said circuit simulator using said simulation deck containing said chosen I/O behavioral model and said operating conditions; and

means for performing I/O floor planning for said I/O circuit based on said received simulation results.

6.   The system of Claim 5, wherein said system further includes means for dynamically analyzing simulation results based on user defined criteria.

7.   The system of Claim 5, wherein said means for collecting further includes means for collecting design specification from a customer's environment condition.

8.   The system of Claim 5, wherein said means for sorting further includes means for sorting said collected design data according to a frequency of operation of said I/O circuit.

9.   (requested to be cancelled) A computer usable medium having a computer program product for performing input/output (I/O) floor planning on an integrated circuit design, said computer usable medium comprising:

program code means for collecting design data related to an I/O circuit of said integrated circuit design from a plurality of libraries, customer specifications and design databases;

program code means for sorting said collected design data for optimizing simulations of said I/O circuit under operating conditions;

program code means for determining whether or not a simulation is required for said I/O circuit before performing I/O floor planning on said I/O circuit;

in response to a determination that a simulation is required on said I/O circuit before performing I/O floor planning on said I/O circuit,

program code means for sending said collected design data to a simulation interface;

program code means for choosing an I/O behavioral model and a package model by said simulation interface based on said collected design data on said I/O circuit;

program code means for dynamically building a simulation deck by said simulation interface using said chosen models along with appropriate operating conditions; and

program code means for receiving simulation results by said simulation interface from a circuit simulator after a simulation had been performed by said circuit simulator using said simulation deck containing said chosen I/O behavioral model and said operating conditions; and

program code means for performing I/O floor planning for said I/O circuit based on said received simulation results.

10.   (requested to be cancelled) The computer usable medium of Claim 9, wherein said computer usable medium further includes program code means for dynamically analyzing simulation results based on user defined criteria.

11.   (requested to be cancelled) The computer usable medium of Claim 9, wherein said program code means for collecting further includes program code means for collecting design specification from a customer's environment condition.

12.   (requested to be cancelled) The computer usable medium of Claim 9, wherein said program code means for sorting further includes means for sorting said collected design data according to a frequency of operation of said I/O circuit.

EVIDENCE APPENDIX

Other than the Office Actions and responses already of record, no additional evidence has been entered by Appellants that is relevant to the present appeal.

RELATED PROCEEDINGS APPENDIX

There is no related proceeding as described by 37 C.F.R. § 41.37(c)(1)(x) known to Appellants, Appellants' legal representative or assignee.